3. Paragraph [0034]

Please replace paragraph [0034] with the following amended paragraph:

[0034] The approach illustrated above may be used to process instructions for wide variety of multi-threaded devices such as a central processing unit (CPU). The approach may also be used to process instructions for a device including multiple processors. As an example, the techniques may be implemented within a development tool for ~~Intel's(r)~~ INTEL's ~~Internet eXchange network Processor~~ INTERNET EXCHANGE PROCESSOR (IXP) processor.

4. Paragraph [0039]

Please replace paragraph [0039] with the following amended paragraph:

[0039] As shown, the network processor 350 features other components including a single-threaded general purpose processor 360 (e.g., a ~~StrongARM(r) XScale(r)~~ STRONGARM XSCALE processor). The processor 350 also includes interfaces 352 that can carry packets between the processor 350 and other network components. For example, the processor 350 can feature a switch fabric interface 352 (e.g., a CSIX interface) that enables the processor 350 to transmit a packet to other processor(s) or circuitry connected to the fabric. The processor 350 can also feature an interface 352 (e.g., a System Packet Interface Level 4 (SPI-4) interface) that enables to the processor 350 to communicate with physical layer (PHY) and/or link layer devices. The processor 350 also includes an interface 358 (e.g., a ~~Peripheral Component Interconnect~~

PERIPHERAL COMPONENT INTERCONNECT (PCI) bus interface) for communicating, for example, with a host.